504 and 506 of FIG. 5, discussed below).

-Please amend the specification at the paragraph beginning at page 7, line 3 as follows:

Delay elements 16, 20-1 to 20-6 include a circuit that produces an output waveform similar to its input waveform, only delayed by a certain amount of time. Delay elements 16, 20-1 to 20-6 may thus include flip-flop chains (or shift registers), transmission gate based delay elements, cascaded inverter based delay elements, voltage-controlled based delay elements, etc. FIG. 2 shows an enlarged view of one of input memory banks 14 of the internal memory organization scheme 10. The smaller elements represent one-cycle delay elements 16, 20-1 to 20-6. Since each input memory bank ~~14~~ 14-2 to 14-11 is dual-ported, there are two separate data paths 26, 28 exiting each input memory bank ~~14~~ 14-2 to 14-11 and entering delay elements 16.

-Please amend the specification at the paragraph beginning at page 7, line 10 as follows:

Computation engines ~~12~~ 12-1 to 12-6 include logic circuitry that takes data from input memory banks ~~14~~ 14-1 to 14-11, ~~18~~ 18-1 to 18-6 and delay elements 16, 20-1 to 20-6 perform ~~performs~~ FDTD calculations on this data, and outputs the results to output memory banks ~~22~~ 22-1 to 22-6.

-Please amend the specification at the paragraph beginning at page 7, line ~~23~~ 13 as follows:

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Although the internal memory organization scheme 10 of FIG. 1 shows distinct numbers of memory banks ~~14~~ 14-1 to 14-11, ~~18~~ 18-1 to 18-6, ~~22~~ 22-1 to 22-6, delay elements 16, 20-1 to 20-6 and computation engines ~~12~~ 12-1 to 12-6, the present invention is not limited to these distinct numbers. Rather, the internal memory organization scheme 10 may include more or less memory banks ~~14~~ 14-1 to 14-11, ~~18~~ 18-1 to 18-6, ~~22~~ 22-1 to 22-6, delay elements 16, and computation engines ~~12~~ 12-1 to 12-6 than are shown in FIG. 1.